DO NOT ENTER TM 12/20/04

U.S. Pat. Appl. 09/926,320

AMENDMENTS TO THE CLAIMS:

Claim 1-16 (canceled)

17. (new) A computer system for processing stack-based instructions, comprising:

a register file that has entries each designed to be able to hold a word of data;

an advanced pointer stack that has entries each designed to be able to hold an entry address in said register file and that, in combination with said register file, is to virtually configure uppermost part of the operand stack grounded on all the issued instructions;

a completed pointer stack that has entries each designed to be able to hold an entry address in said register file and that, in combination with said register file, is to virtually configure uppermost part of the operand stack grounded on all the completed instructions;

a data buffer that has entries each designed to be able to hold a word of data and that can hold lower operand-stack elements that are common to said two operand stacks;

an instruction buffer that is a FIFO queue for holding substances of instructions that have been already issued but not yet completed; and

means for executing operations involved in issued instructions out of order;

wherein, in the course of issue of an instruction / a group of instructions,